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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/889,798	07/20/2001	Hiroshi Hatae	520.40265X00	8803

7590 06/15/2004

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EXAMINER
O BRIEN, BARRY J

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/889,798	HATAE ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2001 and 21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Copy of Declaration as received on 12/21/01.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The abstract of the disclosure is objected to because of the following:

   a. The abstract contains reference numerals without specifying a figure to which they refer, which is improper. Please remove the reference numerals from the abstract language.

   b. The "address bus" in the abstract is referred to by reference number "18", although in all the drawings the "address bus" is referenced by number "10". Please correct the abstract language.

   Correction is required. See MPEP § 608.01(b).

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Although a new title is listed on the 35 U.S.C. 371 paperwork, it is not the title that was on the instant application's corresponding PCT case. Thus the original title, "Data processor and device for arithmetic operation" is the current title of the instant application. If the Applicant would like the title listed on the 35 U.S.C. 371 paperwork to be the title of the instant application, namely, "Parallel processing device for image data with SIMD ALU", then the title must be officially amended by the Applicant.

Claim Objections

7. Claims 2, 7, 9, 15-17 and 19-20 are objected to because of the following informalities:

a. Claim 2 recites the limitation, "SIDM type" on its third line. Please amend the limitation to correctly read, "SIMD type". See also similar corrections that need to be made in claims 15, 17 and 19.

b. Claim 7 recites the limitation, "parallely" on its fourth line. This is not grammatically correct English, nor a correct English word. Please correct the claim language to more appropriately use the term, perhaps by changing the claim language to incorporate the phrase "in parallel".

c. Claim 9 recites the limitation, "The data processor for image processing according to claim 8" on its first and second lines. There is a lack of antecedent basis for this preamble. Please correct it to read, "The data processor according to claim 8" in order to provide the correct antecedent basis for the claim.

d. Claim 9 recites the limitation, "the degree of approximation". There is a lack of antecedent basis for this limitation in the claims. Please correct it to read, "a degree of approximation" in order to provide the correct antecedent basis for the claim.

e. Claim 15 recites the limitation, "claim14" on its first line. Please correct the limitation to more clearly read, "claim 14". See also similar corrections that need to be made in claims 17, 19 and 20.

f. Claim 15 recites the limitation, "A data processor according to claim 14" on its first line. Please correct this limitation to more clearly read, "The data processor according to claim 14". See also similar corrections that need to be made in claims 17, 19 and 20.

g. Claim 16 recites the limitation, "storage means connected with said CPU by address bus" on its third and fourth lines. Please correct the claim language to more clearly read, "storage means connected with said CPU by an address bus".

h. Claim 16 recites the limitation, "A data processor comprising;" on its first line. Please correct the claim language to more clearly read, "A data processor comprising:".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 8-9 and 11-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10. Claim 8 recites the limitation, "applying all the bit widths". While the specification describes the copying/shifting of various sets of bits in registers (see pgs. 9-11 of specification), there is no mention of "apply" a "bit width" to any registers. For the purposes of this examination, the Examiner will assume that "applying" bit widths refers to copying data of a certain width from one register into another register. Dependent claim 9 is rejected for the same reasons as above, as it includes the limitations of its parent claim.

11. Claim 11 recites the limitation, "supplying a bit width". While the specification describes the copying/shifting of various sets of bits in registers (see pgs. 9-11 of specification), there is no mention of "supplying" a "bit width" to any registers. For the purposes of this examination, the Examiner will assume that "supplying" bit widths refers to copying data of a certain width from one register into another register. Dependent claim 13 is rejected for the same reasons as above, as it includes the limitations of its parent claim.

12. Claim 12 recites the limitation, "supplying the bit width". While the specification describes the copying/shifting of various sets of bits in registers (see pgs. 9-11 of specification), there is no mention of "supplying" a "bit width" to any registers. For the purposes of this examination, the Examiner will assume that "supplying" bit widths refers to copying data of a

certain width from one register into another register. Dependent claim 13 is rejected for the same reasons as above, as it includes the limitations of its parent claim.

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 1-9, 11-12 and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. Claim 1 recites the limitation, "A local data bus". It is unclear what this data bus is "local" to, as the claim language does not define if it is local to the data processor, the ALU, the CPU, or something else altogether. Please correct the claim language to more clearly define the metes and bounds of the claim. Dependent claims 2-9 are rejected for the same reasons as above, as they include the limitations of their parent claims.

16. Claim 4 recites the limitation, "and controlling data transfer between the first and second memories" on its fourth and fifth lines. It is unclear what limitation in the claim is actually performing the "controlling", as the claim language does not define if it is the first storage means, the DMA circuit, or something else altogether. Please correct the claim language to more clearly define the metes and bounds of the claim. Dependent claims 5-6 and 8-9 are rejected for the same reasons as above, as they include the limitations of their parent claims.

17. Claim 8 recites the limitation, "supplying the bit width of the first input terminal of said processor element from the most significant bit". It is unclear how a single bit can represent the width of an entire bus. Please correct the claim language to more clearly define the metes and bounds of the claim. Claims 11 and 12 require similar corrections, and are thus rejected for the

same reasons as above. Dependent claims 9 and 13 are rejected for the same reasons above, as they include the limitations of their parent claims.

18. Claim 18 recites the limitation, "a first storage means stored instructions" on its second line. It is unclear what this limitation means, and appears to be a typographical error. Please correct the claim language to more clearly read, "a first storage means". For the purposes of this examination, the Examiner will assume that it was, in fact, a typographical error, and that the limitation refers to simply a "first storage means". Dependent claims 19 and 20 are rejected for the same reasons as above, as they include the limitations of their parent claims.

19. Claim 20 recites the limitation " said second memories " in its third and fourth lines. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, the Examiner will assume that this refers to the "second storage means" claimed in parent claim 18.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

21. Claims 1-8, 10-12 and 14-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Morton, U.S. Patent No. 5,822,606.

22. Regarding claim 1, Morton has taught a data processor comprising:

a. A first arithmetic and logic unit (see 110 of Fig.1, and 806 of Fig.8) controlled by a CPU (see 105, 107 of Fig.1, Col.7 lines 33-50 and Col.17 lines 20-23),

b. First storage means (501 of Fig.5),

c. A local data bus (116 of Fig.1, 502 of Fig.5) having a bus width wider than a data bus width of said CPU, and connecting the first arithmetic and logic unit and the first storage means (see Fig.5). Here, data bus (116 of Fig.1) is 32 bits wide (see Col.10 lines 3-8), while a data bus of the CPU is only 24 bits wide (see 616 of Fig.6).

d. An address bus (127 of Fig.1) commonly connected to said CPU, the first arithmetic and logic unit, and said first storage means (see Fig.1 and Col.20 lines 5-16).

23. Regarding claim 2, Morton has taught the data processor according to claim 1, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIMD type (see Col.7 lines 3-9 and Col.14 lines 1-12).

24. Regarding claim 3, Morton has taught the data processor according to claim 1, wherein a plurality of said first arithmetic and logic units are arranged in parallel (see 110-113 of Fig.1).

25. Regarding claim 4, Morton has taught the data processor according to claim 1, wherein said first storage means has a first memory (501 of Fig.5), a second memory (202 of Fig.2), and a DMA circuit (201 of Fig.2) connected to said address bus and said data bus and controlling data transfer between the first and second memories. Here, the DMA controller (201 of Fig.2) is connected to both the SDRAM via the internal data bus (117 of Fig.1,2, see Col.13 lines 41-43)

and the DMA Buffer (202 of Fig.2) via the internal control bus (127 of Fig.1,2), and controls data transfer between them (see Col.10 lines 60-67).

26. Regarding claim 5, Morton has taught the data processor according to claim 4, wherein said first storage means has means for performing sign extension when data is transferred from said second memory to said first memory by the DMA circuit (see Col.10 lines 3-7). Here, data is sign extended from 32 to 64 bits en route from the SDRAM (501 of Fig.5) to the DMA buffer (202 of Fig.2).

27. Regarding claim 6, Morton has taught the data processor according to claim 4, wherein said first memory has first (501 of Fig.5) and second (104 of Fig.1) work memories, and said first storage means further comprises means for alternately switching between connection of the first and second work memories to said first arithmetic and logic unit and said second memory, respectively, and connection of the first and second work memories to said second memory and said first arithmetic and logic unit, respectively (see Col.10 lines 60-67 and Col.13 lines 41-43). Here, the internal control bus is able to arbitrate connections between the ALU's (110-113 of Fig.1) and the DMA buffer (202 of Fig.2).

28. Regarding claim 7, Morton has taught the data processor according to claim 1, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIMD control type (see Col.7 lines 3-9 and Col.14 lines 1-12) for parallely performing arithmetic process of plural data by a single instruction from said CPU (see Col. 7 lines 33-50).

29. Regarding claim 8, Morton has taught the data processor according to any one of claims 1 to 7, wherein said first arithmetic and logic unit taking the form of an SIMD control type arithmetic and logic unit (see Col.7 lines 3-9 and Col.14 lines 1-12), comprising:

a. A plurality of processor elements (110-113 of Fig.1) each having a first input terminal (815 of Fig.8), a second input terminal (128 of Fig.1), and a first output terminal (see 816 of Fig.8) and operated by a control signal (127 of Fig.1) from said CPU,

b. A first register (202 of Fig.2) having a bit width equal to a total of bit widths of input terminals of all of first input terminals of said plurality of processor elements (see Col.11 lines 20-24). Here, the FIFO buffer is organized as rows of 8 bytes (64 bits) that can each be considered a register, each of which is equal to the sum of the widths of the first input terminals of the four processor elements, each of which are 16 bits (see Fig.1).

c. A second register (202 of Fig.2) having a bit width equal to a total of bit widths of second input terminals of all of said plurality of processor elements and applying all the bit widths to the second input terminals of all the processor elements without an overlap (see Col.11 lines 20-24). Here, the FIFO buffer is organized as rows of 8 bytes (64 bits) that can each be considered a register, each of which is equal to the sum of the widths of the first input terminals of the four processor elements, each of which are 16 bits (see Fig.1).

d. A third register (207 of Fig.2) having a bit width equal to or wider than a bit width of the second input terminal of each of said processor elements and capable of shifting data to the second register on a unit basis of the bit width of the second input terminal (see Col.11 lines 50-58). Here, the register has a bit width of 16

bits, which is equal to the bit width of a single processing element input terminal, and shifts the entire register contents into one of the 'registers' of the FIFO.

e. A selector for selecting data of said first register and supplying the bit width of the first input terminal of said processor element from the most significant bit commonly to the first input terminals of all of said processor elements (see Col.10 lines 50-59). Here, data of width equal to the input of a processing element (16 bits) is selected from the most significant (i.e. first in of a FIFO) bits of one of the 'registers' of the FIFO and sent to the processing elements input via the memory bus (117 of Fig.1).

f. A write control circuit (101 of Fig.1) controlled by said address bus, for writing data to said first, second, and third registers via said local bus (see Fig.1),

g. A circuit (116 of Fig.1) for outputting data of said output terminal to said local data bus (see Col.9 lines 60-64).

30. Regarding claim 10, Morton has taught an arithmetic and logic unit of an SIMD control type (see Col.7 lines 3-9 and Col.14 lines 1-12), comprising:

a. A plurality of processor elements (110-113 of Fig.1), each having a first input terminal (815 of Fig.8), a second input terminal (128 of Fig.1), and a first output terminal (see 816 of Fig.8),

b. A first register (202 of Fig.2) having a bit width equal to a total of bit widths of first input terminals of all of said plurality of processor elements (see Col.11 lines 20-24). Here, the FIFO buffer is organized as rows of 8 bytes (64 bits) that can each be considered a register, each of which is equal to the sum of the widths of

the first input terminals of the four processor elements, each of which are 16 bits (see Fig.1).

c. A second register (202 of Fig.2) having a bit width equal to a total of bit widths of second input terminals of all of said processor elements (see Col.11 lines 20-24). Here, the FIFO buffer is organized as rows of 8 bytes (64 bits) that can each be considered a register, each of which is equal to the sum of the widths of the first input terminals of the four processor elements, each of which are 16 bits (see Fig.1).

d. A third register (207 of Fig.2) having a bit width equal to or wider than a bit width of the second input terminal of said processor element and capable of shifting data to the second register on a unit basis of the bit width of the second input terminal (see Col.11 lines 50-58). Here, the register has a bit width of 16 bits, which is equal to the bit width of a single processing element input terminal, and shifts the entire register contents into one of the 'registers' of the FIFO.

31. Regarding claim 11, Morton has taught the SIMD control type arithmetic and logic unit according to claim 10, wherein said first register has a connection circuit (128 of Fig.1) for commonly supplying a bit width of a first input terminal of said processor element from the most significant bit to all of said processor elements, and a connection circuit for supplying all of bit widths so as not to be overlapped to all of the processor elements (see Col.11 lines 50-58). Here, the FIFO (which contains the 'first' and 'second' registers) can transmit data of width 64 bits, such that separate 16 bits of data go to each of the four processing units (see Fig.1).

32. Regarding claim 12, Morton has taught the SIMD control type arithmetic and logic unit according to claim 10, further comprising:

a. A selector for supplying the bit width of the first input terminal of said processor element from the most significant bit of said first register to all of said processor elements (see Col.10 lines 50-59). Here, data of width equal to the input of a processing element (16 bits) is selected from the most significant (i.e. first in of a FIFO) bits of one of the 'registers' of the FIFO and sent to the processing elements input via the memory bus (117 of Fig.1).

b. Means for performing, every clock, an arithmetic process in said processor element (see Col.27 lines 25-43), a data shifting process on the unit basis of the bit width of the first input terminal of said processor element in said first register, and a data shifting process on the unit basis of the bit width of the second input terminal of said processor element in said second and third registers (see Col.11 lines 50-59). Here, because the two input terminals of the processing element are each 16 bits, and because data coming from the third register is double clocked (see Col.11 lines 50-59, data corresponding to the width of both the first and second input terminals can be shifted into the first and second registers from the third register every clock cycle.

33. Regarding claim 14, Morton has taught a data processor having a CPU (see 105, 107 of Fig.1, Col.7 lines 33-50 and Col.17 lines 20-23), a first arithmetic unit (see 110 of Fig.1, and 806 of Fig.8), storage means (501 of Fig.5), an address bus (127 of Fig.1) connecting said CPU and said storage means (see Fig.1 and Col.20 lines 5-16), and a local data bus (116 of Fig.1, 502 of

Fig.5) connecting the first arithmetic unit and the storage means (see Fig.1 and Col.20 lines 5-16), wherein said CPU comprises an instruction decode circuit decoding an instruction (see Col.17 lines 20-30), output of which controls said first arithmetic unit (see Col.17 lines 33-67), and said local data bus having a bus width wider than a data bus width. Here, data bus (116 of Fig.1) is 32 bits wide (see Col.10 lines 3-8), while a data bus of the CPU is only 24 bits wide (see 616 of Fig.6).

34. Regarding claim 15, Morton has taught the data processor according to claim 14, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIMD type (see Col.7 lines 3-9 and Col.14 lines 1-12).

35. Regarding claim 16, Morton has taught a data processor comprising:

a. A CPU (see 105, 107 of Fig.1, Col.7 lines 33-50 and Col.17 lines 20-23),

b. A first arithmetic and logic unit controlled by said CPU (see 110 of Fig.1, and 806 of Fig.8),

c. Storage means (see 501 of Fig.5, Fig.1 and Col.20 lines 5-16) connected with said CPU by address bus (see 127 of Fig.1 and Col.20 lines 5-16),

d. A DMA circuit (201 of Fig.2) connected with said address bus and said storage means. Here, the DMA controller (201 of Fig.2) is connected to both the SDRAM via the internal data bus (117 of Fig.1,2, see Col.13 lines 41-43), and the DMA Buffer (202 of Fig.2) via the internal control bus (127 of Fig.1,2), and controls data transfer between them (see Col.10 lines 60-67).

e. A local data (116 of Fig.1) bus having a bus width wider than a data bus width of said CPU and connecting the arithmetic and logic unit and the storage means (see

Fig.5). Here, data bus (116 of Fig.1) is 32 bits wide (see Col.10 lines 3-8), while a data bus of the CPU is only 24 bits wide (see 616 of Fig.6).

36. Regarding claim 17, Morton has taught the data processor according to claim 16, wherein said first arithmetic and logic unit is an arithmetic and logic unit of an SIMD type (see Col.7 lines 3-9 and Col.14 lines 1-12).

37. Regarding claim 18, Morton has taught a data processor comprising:

a. A first storage means stored instructions (604 of Fig.6),

b. A CPU (see 105, 107 of Fig.1, Col.7 lines 33-50 and Col.17 lines 20-23) connected with said first storage means through an address bus (127 of Fig.1) and a first data bus (616 of Fig.6),

c. A second storage means (see 501 of Fig.5, Fig.1 and Col.20 lines 5-16) connected with said CPU through said address bus (see 127 of Fig.1 and Col.20 lines 5-16),

d. An arithmetic and logic unit (see 110 of Fig.1, and 806 of Fig.8) connected with said second storage means through an second data bus (116 of Fig.1, 502 of Fig.5, and see Fig.1 and Col.20 lines 5-16) having bus width wider than data bus width of said first data bus. Here, data bus (116 of Fig.1) is 32 bits wide (see Col.10 lines 3-8), while a data bus of the CPU is only 24 bits wide (see 616 of Fig.6).

38. Regarding claim 19, Morton has taught a data processor according to claim 18, wherein said arithmetic and logic unit is an arithmetic and logic unit of an SIMD type (see Col.7 lines 3-9 and Col.14 lines 1-12).

39. Regarding claim 20, Morton has taught a data processor according to claim 18 or 19, which further comprises a DMA circuit (201 of Fig.2) connected to said address bus, said first

data bus, and said second memories. Here, the DMA controller (201 of Fig.2) is connected to both the SDRAM (501 of Fig.5) via the internal data bus (117 of Fig.1,2, see Col.13 lines 41-43) and the DMA Buffer (202 of Fig.2) via the internal control bus (127 of Fig.1,2).

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claims 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton, U.S. Patent No. 5,822,606 as applied to claims 8, and 11 or 12, respectively, above, and further in view of Horishi et al., U.S. Patent No. 6,115,073.

42. Regarding claim 9, Morton has taught the data processor for image processing according to claim 8, but has not explicitly taught wherein said processor element is an arithmetic and logic circuit for adding up a subtraction value of data of said first and second input terminals for a predetermined range and outputting resultant data, data is stored in a plurality of pixels of an image to be encoded in said first register, data of a plurality of pixels of a reference image to be referred to is stored in said second register, and outputs of said plurality of processor elements are taken as the degree of approximation correspond to a plurality of motion vectors.

43. However, Horishi has taught a circuit for inputting a first and second pixel data values stored in first and second registers (see Horishi, Col.6 lines 22-35) so the sum of the absolute value of their differences can be accumulated (see Horishi, Col.8 line 34 – Col.9 line 23) and

represent a degree of approximation corresponding to the motion vector defined by the pixel data values (see Horishi, Col.10 lines 18-34). This circuit helps improve the conversion of the pixel data to a higher quality while decreasing the space needed for storing coefficients of the pixel data (see Horishi, Col1 lines 39-60). Morton has taught a data processor for processing pixel data corresponding to video data (see Morton, Col.38 lines 23-52). Therefore, one of ordinary skill in the art would have found it obvious to modify the data processor of Morton to input first and second pixel data values into first and second registers, and subsequently summing the absolute value of their differences, thus representing a degree of approximation of a motion vector so that the processor can improve its conversion of the pixel data to a higher quality while decreasing the space needed for storing data coefficients.

44. Regarding claim 13, Morton has taught the SIMD control type arithmetic and logic unit according to claim 11 or 12, used for image processing, but has not explicitly taught wherein:

a. Data of a plurality of pixels in a first image is stored in said first register,

b. Data of a plurality of pixels in a second image is stored in said second and third registers,

c. Said processor element takes the form of an arithmetic and logic circuit for accumulating a difference between data applied from said first input terminal and data applied from said second input terminal,

d. Means for outputting the degree of approximation corresponding to a plurality of motion vectors between said first and second images from each of said plurality of processor elements is provided.

45. However, Horishi has taught a circuit for inputting a first and second pixel data values stored in first and second registers (see Horishi, Col.6 lines 22-35) so the sum of the absolute value of their differences can be accumulated (see Horishi, Col.8 line 34 – Col.9 line 23) and represent a degree of approximation corresponding to the motion vector defined by the pixel data values (see Horishi, Col.10 lines 18-34). This circuit helps improve the conversion of the pixel data to a higher quality while decreasing the space needed for storing coefficients of the pixel data (see Horishi, Col1 lines 39-60). Morton has taught a data processor for processing pixel data corresponding to video data (see Morton, Col.38 lines 23-52). Therefore, one of ordinary skill in the art would have found it obvious to modify the data processor of Morton to input first and second pixel data values into first and second registers, and subsequently summing the absolute value of their differences, thus representing a degree of approximation of a motion vector so that the processor can improve its conversion of the pixel data to a higher quality while decreasing the space needed for storing data coefficients.

Conclusion

46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

47. Fry et al., U.S. Patent No. 5,506,957, has taught a processor with an ALU controlled by a CPU with a data bus connecting the ALU and storage means, and an address bus connecting the CPU, the ALU and the storage means.

48. Davies, U.S. Patent No. 5,450,604, has taught a processor with parallel ALU units controlled by a separate control circuit with a shared data bus.

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

50. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
6/10/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

REVISED AMENDMENT PRACTICE: 37 CFR 1.121 CHANGED COMPLIANCE IS MANDATORY - Effective Date: July 30, 2003

All amendments filed on or after the effective date noted above must comply with revised 37 CFR 1.121. See Final Rule: **Changes To Implement Electronic Maintenance of Official Patent Application Records** (68 *Fed. Reg.* 38611 (June 30, 2003), posted on the Office's website at: http://www.uspto.gov/web/patents/ifw/ with related information. The amendment practice set forth in revised 37 CFR 1.121, and described below, replaces the voluntary revised amendment format available to applicants since February 2003. **NOTE: STRICT COMPLIANCE WITH THE REVISED 37 CFR 1.121 IS REQUIRED AS OF THE EFFECTIVE DATE (July 30, 2003).** The Office will notify applicants of amendments that are not accepted because they do not comply with revised 37 CFR 1.121 via a Notice of Non-Compliant Amendment. See MPEP 714.03 (Rev. 1, Feb. 2003). The non-compliant section(s) will have to be corrected and the entire corrected section(s) resubmitted within a set period.

Bold underlined italic font has been used below to highlight the major differences between the revised 37 CFR 1.121 and the voluntary revised amendment format that applicants could use since February, 2003.
Note: The amendment practice for **reissues** and **reexamination proceedings**, except for drawings, has not changed.

REVISED AMENDMENT PRACTICE

I. Begin each section of an amendment document on a separate sheet:
Each section of an amendment document (*e.g.*, Specification Amendments, Claim Amendments, Drawing Amendments, and Remarks) must begin on a separate sheet. Starting each separate section on a new page will facilitate the process of separately indexing and scanning each section of an amendment document for placement in an image file wrapper.

II. Two versions of amended part(s) no longer required:
37 CFR 1.121 has been revised to no longer require two versions (a clean version and a marked up version) of each replacement paragraph or section, or amended claim. Note, however, the requirements for a clean version and a marked up version for substitute specifications under 37 CFR 1.125 have been retained.

A) Amendments to the claims:
Each amendment document that includes a change to an existing claim, cancellation of a claim or submission of a new claim, **must include a complete listing** of all claims in the application. After each claim number in the listing, the status must be indicated in a parenthetical expression, and **the text of each pending claim** (with markings to show current changes) must be presented. The claims in the listing will replace all prior claims in the application.

(1) The current status of all of the claims in the application, including any previously canceled, not entered or withdrawn claims, must be given in a parenthetical expression following the claim number using only one of the following seven status identifiers: (original), (currently amended), (canceled), (withdrawn), (new), ***(previously presented) and (not entered).*** The text of all pending claims, ***including withdrawn claims,*** must be submitted each time any claim is amended. Canceled ***and not entered*** claims must be indicated by only the claim number and status, without presenting the text of the claims.

(2) The text of all claims being currently amended must be presented in the claim listing with markings to indicate the changes that have been made relative to the immediate prior version. The changes in any amended claim must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** (e.g., ~~number 4 as~~ number 14 as). An accompanying clean version is not required and should not be presented. Only claims of the status "currently amended," and "withdrawn" that are being amended, may include markings.

(3) The text of pending claims not being currently amended, ***including withdrawn claims,*** must be presented in the claim listing in clean version, *i.e.*, without any markings. Any claim text presented in clean version will constitute an assertion that it has not been changed relative to the immediate prior version except to omit markings that may have been present in the immediate prior version of the claims.

(4) A claim being canceled must be listed in the claim listing with the status identifier "canceled"; the text of the claim must not be presented. Providing an instruction to cancel is optional.
(5) Any claims added by amendment must be presented in the claim listing with the status identifier "(new)"; the text of the claim must not be underlined.
(6) All of the claims in the claim listing must be presented in ascending numerical order. Consecutive canceled, or not entered, claims may be aggregated into one statement (*e.g.*, Claims 1 – 5 (canceled)).

Example of listing of claims (use of the word "claim" before the claim number is optional):

Claims 1-5 (canceled)

Claim 6 (previously presented): A bucket with a handle.

Claim 7 (withdrawn): A handle comprising an elongated wire.

Claim 8 (withdrawn): The handle of claim 7 further comprising a plastic grip.

Claim 9 (currently amended): A bucket with a ~~green~~ blue handle.

Claim 10 (original): The bucket of claim 9 wherein the handle is made of wood.

Claim 11 (canceled)

Claim 12 (not entered)

Claim 13 (new): A bucket with plastic sides and bottom.

B) Amendments to the specification:
Amendments to the specification, including the abstract, must be made by presenting a replacement paragraph or section or abstract marked up to show changes made relative to the immediate prior version. An accompanying clean version is not required and should not be presented. Newly added paragraphs or sections, including a new abstract (instead of a replacement abstract), must not be underlined. A replacement or new abstract must be submitted on a separate sheet, 37 CFR 1.72. If a substitute specification is being submitted to incorporate extensive amendments, both a clean version (which will be entered) and a marked up version must be submitted as per 37 CFR 1.125.

The changes in any replacement paragraph or section, or substitute specification must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as)*

C) Amendments to drawing figures:
Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment, ***and may be accompanied by a marked-up copy of one or more of the figures being amended, with annotations.*** Any replacement drawing sheet must ***be identified in the top margin as "Replacement Sheet"*** and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. ***Any marked-up (annotated) copy showing changes must be labeled "Annotated Marked-up Drawings" and accompany the replacement sheet in the amendment (e.g., as an appendix).*** The figure or figure number of the amended drawing(s) must **not** be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Questions regarding the submission of amendments pursuant to the revised practice set forth in this flyer should be directed to: Elizabeth Dougherty or Gena Jones, Legal Advisors, or Joe Narcavage, Senior Special Projects Examiner, Office of Patent Legal Administration, by e-mail to patentpractice@uspto.gov or by phone at (703) 305-1616.